RACORS Processors General Properties

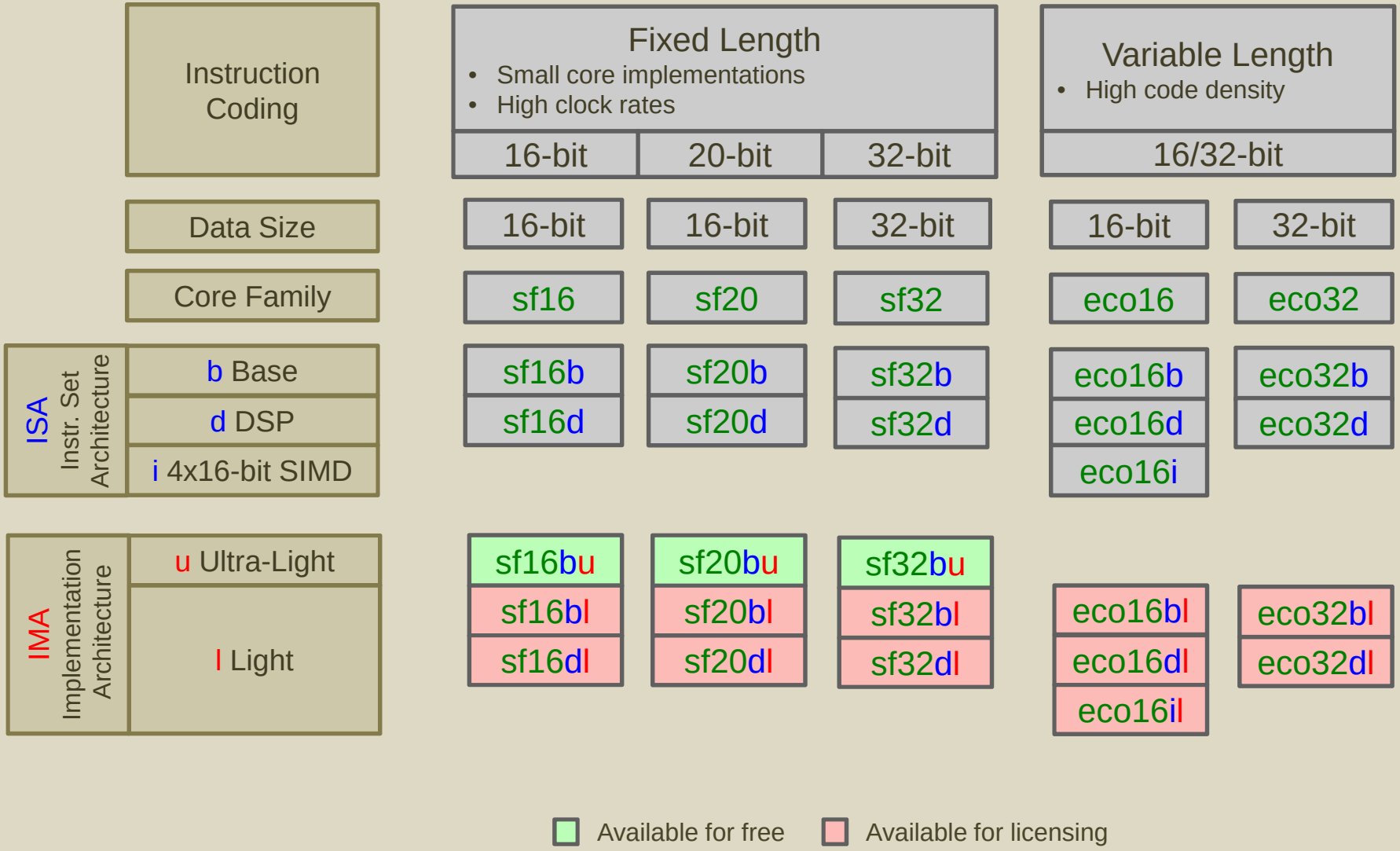
- Families
  - Five families: eco16, eco32, sf16, sf20 and sf32
  - The eco families have variable length instruction coding and are focused on high code density
  - The sf families have fixed length instr. coding and are focused on small core size and high clock rates
  - eco16, sf20 and sf16 have 16-bit registers and support 8/16-bit native data types
  - eco32 and sf32 have 32-bit registers and support 8/16/32-bit native data types

- ISA (Instruction Set Architecture)
  - The ISA defines the programming model (registers, instruction set, …)
  - Each family has a b (base) ISA for general purpose control & computing, all cores of a family support the base ISA instruction set
  - For higher performance and DSP requirements single and multi-way DSP extension ISAs are available

- IMA (Implementation Architecture)
  - All implementations of an ISA are binary compatible
  - IMA properties determine the performance and resource consumption of a core
  - IMA properties include: pipeline-depth, bus-width, parallel execution units, performance enhancement features like loop-caches, branch target caches, etc.

- DSP Precision
  - All DSP extension ISAs include a precision enhancement feature (patented). Sum-of-Product computations are done with twice the precision of the accumulator register (general-purpose) without adding registers or instructions to the programming model

Family/ISA/IMA Hierarchy



Properties of available cores

Core	Size [kgates]	Size [LEs]	Max Clock	Instr. Bus	Data Bus	Sec	Target Applications
sf16bu	10	1350 (*)	120	16	16	no	General Purpose Control & Computing 128kb/64kb instr./data address space
sf16bl	15	2350	130	16	16	no	
sf16dl	20	3200	130	16	16	no	Low end DSP, e.g. servo, speech,…, 32-bit accumulation
sf20bu	10	1500 (*)	120	20	16	no	General Purpose Control & Computing 64kx20-bit instr. addr. Space, 64kBytes data addr. space
sf20bl	16	2750	130	20	16	no	
sf20dl	20	3300	130	20	16	no	Low end DSP, e.g. servo, speech,…, 32-bit accumulation
sf32bu	15	2300 (*)	110	32	32	yes	General Purpose Control & Computing, secure systems 4Gb/4Gb instr./data address space
sf32bl	30	5600	110	32	32	yes	
sf32dl	50	7500	100	32	32	yes	High precision DSP, 64-bit accumulation
eco16bl	25	5400	100	32	16	no	Gen. Purp. Ctr. & Comp.,4Mb/64kb instr./data
eco16dl	35	6500	100	32	16	no	16-bit DSP, e.g. servo, low-end audio,…, 32-bit accum.
eco16il	80	13700	100	32	2 x 64	no	image processing, video, 4-way SIMD
eco32bl	40	7700	100	32	32	yes	Gen. Purp. Ctr. & Comp.,4Gb/4Gb instr./data, sec. sys.
eco32dl	60	9300	100	32	32	yes	High precision DSP/audio, 64-bit accumulation

Size [kgates] Estimate for Std-Cells, total area divided by the area of a medium-drive 2-input NAND gate
Size[LEs] Average synthesis result for low-end FPGAs (Logic Elements, LUTs)
Max Clock Average synthesis result for low-end FPGAs [MHz], significantly higher clocks possible for Std-Cells and high-end FPGAs
Sec System/Application modes with possible hardware protection of memory areas in system mode, for secure systems
(*) One additional block RAM (FPGA) or compiled RAM/Reg.-File (Std-Cell) required